ABSTRACT OF THE DISCLOSURE

It was difficult to precisely estimate a layout area of a logic circuit diagram from the logic circuit diagram.

Then, in order to estimate the layout area from the logic circuit diagram constituted by a transistor as a minimum unit, there is provided with hierarchy developing means for developing logic circuit diagram information having a hierarchical structure to information at a transistor level, configuration parameter information extracting means for extracting information such as a gate length, a gate width or the like of each transistor, area calculating means for calculating each transistor area using an area calculation formula for calculating a transistor area from the above information, and layout area estimating means for obtaining a layout area by adding all areas of the transistors together.